WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

first and second wells opposite in conductivity type and adjacent to each other;

a well isolation structure in form of a shallow trench formed on the boundary of said first and second wells, said well isolation structure having a first width and a second width larger than the first isolation width;

a first device region provided in said first well; and

a second device region provided in said second well,

wherein said first and second device regions are provided so as to be opposed at said first width of said well isolation structure and wherein said first and second device regions do not meet facing at said second width of said well isolation structure.

2. The semiconductor device according to claim 1, wherein one of said opposed device regions is a dummy device region unnecessary for an actual circuit, and has a width at least equal to that of the other device region.

3. The semiconductor device according to claim 2, wherein said dummy device region has the same conductivity type as that of the well in which it is formed.

4. The semiconductor device according to claim 2, wherein said dummy device region has the opposite conductivity type from that of the well in which it is formed.

5. The semiconductor device according to claim 1, wherein when both of said device regions are not equal in width and at least one of said opposed device regions requires a fine device isolation structure, the other device region has a width capable of confronting the former device region over the full width of the former device region.

6. The semiconductor device according to claim 5, wherein said other device region includes a dummy device region provided to at least one end of the other device region, said dummy device region ensuring necessary confronting length.

7. The semiconductor device according to claim 6, wherein the conductivity of the dummy device region is the same as the conductivity of the other device region.

8. The semiconductor device according to claim 1, wherein opposed device regions are cell patterns of static RAM, and a well isolation structure having a narrower width than other circuit blocks is used.

9. A method of manufacturing semiconductor device comprising:

forming a first well of a first conductivity and and a second well of a second conductivity which is opposite to the first conductivity in a manner they are disposed adjacent to each other;

forming a well isolation structure in a form of a shallow trench on the boundary of said first and second wells, said well isolation structure having a first width and a second width which is larger than the first width;

forming a first device region in said first well; and

forming a second device region provided in said second well,

wherein said first and second device regions are provided so as to be opposed at said first width of the well isolation structure and wherein said first and second device regions do not meet facing at the second width of said well isolation structure.

10. The method of manufacturing semiconductor device according to claim 9, wherein one of said first and second device region is provided as a dummy device region unnecessary for an actual circuit, if there is no opposed device regions,

a width of the dummy device region having at least equal to that of the opposing device region.

11. The method of manufacturing semiconductor device according to claim 10, wherein said dummy device region is doped to have the same conductivity type as that of the well in which it is formed.

12. The method of manufacturing semiconductor device according to claim 10, wherein said dummy device region is doped to have the opposite conductivity type from that of the well in which it is formed.

13. The method of manufacturing semiconductor device according to claim 9, wherein when both of said device regions are not equal in width and at least one of said opposed device regions requires a fine device isolation structure, the other device region is made to have a width capable of confronting the former device region over the full width of the former device region.

14. The method of manufacturing semiconductor device according to claim 13, wherein said other device region includes a dummy device region provided to at least one end of the other device region, said dummy device region ensuring necessary confronting length.

15. The method of manufacturing semiconductor device according to claim 10, wherein said dummy device region is doped to have the same conductivity type as that of the other device region.